

N-nary optical semiconductor photonic transistor

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Abstract. In this paper we present a novel optoelectronic device, called a photonic transistor, and we investigate its properties as they pertain to digital electronic applications. The photonic transistor design is based on a heterojunction configuration similar to a semiconductor optical amplifier, and can be used to construct either N-nary digital logic gates or binary Boolean logic gates. The properties of the photonic transistor are investigated using computer simulations, and the numerical results indicate that such a device can be successfully used in digital optoelectronic applications. © 2007 Society of Photo-Optical Instrumentation Engineers. [DOI: 10.1117/1.2802090]

Subject terms: photonic transistor; optical semiconductor amplifier; *N*-valued digital logic; logic gates.

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1 Introduction

Similar to digital electronics, digital photonic circuits and/or chips can be built by using logic gates in which light signals—instead of electrical ones—are used to drive the device. When using light signals, we have two dimensions available for information encoding and computing, namely, the intensity of the optical signal and its wavelength. In other words, we can use a number N ($N \geq 1$) of optical signals with different wavelengths that could each have either zero intensity to represent the binary 0s, or a preselected high intensity to represent the binary 1s.

For computing purposes, one can use either the intensities to represent information, or the wavelengths, or both. If one uses the intensity of the optical signal for information encoding, then one can have a multiple binary system in which each of the N optical signals has two intensities that correspond, respectively, to the binary 0 and to the binary 1. Furthermore, if $N=1$, i.e. if one uses a single optical signal with a fixed wavelength, the system becomes a single binary system that can perform the same logical functions as any digital electronics system.

If the wavelengths of the signals are used to encode information, then the system must necessarily have $N \geq 2$, becoming an N -valued system in which each optical signal has a fixed intensity and represents one of the N logical values of the digital system. If only two wavelengths are used in such a system, then the system becomes once again a binary system, with one wavelength representing the binary 0 and the other representing the binary 1.

However, if both the intensities and the wavelengths are used for information representation and manipulation, then the system becomes a two-dimensional logic system that could not only provide high computational capacity, but could also be constructed in such a way that the transitional functions among the digital values of the system are simple and can be implemented at the physical level by using optical semiconductor devices.

Based on such considerations, an N -valued digital logic

system has been designed that uses both the optical signal intensity (only two values for the intensities are used) and the optical signal wavelength to define the transition functions between the N logical values of an N -nary (instead of binary) computing system. The system has been called an N -nary Digital Photonic (NDP) system and has been developed by implementing the transition functions through N -nary photonic logic gates.¹ The photonic logic gates that have been used in the construction of this system can be in fact used for the construction of various other N -nary optical digital circuits such as optical random access memories,² and the design of any digital optical devices using such logic gates is similar to the design of binary Boolean digital circuitry.

It is worth noting that N -valued logic is not unique. One can construct different logic systems for different applications.³ The larger the N chosen, the larger the number of logic systems that can be devised. When a logic system is designed for computing purposes, it is required to have two fundamental properties: completeness and implementability. The completeness property implies that the logic defines all the necessary operators (i.e., transition functions) to achieve information storage and data computation, and the implementability property ensures that the logic can be physically implemented by some kind of technology in order to be useful. The NDP system was developed to satisfy both of these requirements, and as far as the implementability condition is concerned, the logic gates—which are the key elements of the system—can be constructed by using a class of new optoelectronic devices called photonic transistors, the description and numerical investigation using computer simulation of which constitutes the main topic of the present paper.

The paper is organized as follows. In Sec. 2 we present an operational and physical description of the photonic transistor, insisting on its function as a logic gate, and we describe briefly the mathematical model used to simulate its properties. In Sec. 3 we present a numerical investigation of the properties of such a device, while in Sec. 4 we focus on the performance of optical AND (O-AND) gate configura-

tions constructed by using photonic transistors. We conclude the paper in Sec. 5 with a brief discussion of our results.

2 The Photonic Transistor

One approach to the construction of N-nary photonic logic gates is to use a device that is capable of implementing on/off switching functions for optical signals in a manner similar to the switching operation of a traditional electronic transistor. Furthermore, and based on the operational requirements of the NDP system, the switching capabilities of this device should be controlled by an optical signal and should cover a domain of wavelengths wide enough to allow for the practical implementation of N-nary logic.

With such a device, one can then construct the photonic gates that are necessary for the operational and practical implementation of the N-nary digital logical system described earlier. Due to the operational analogy of such a device with its electronic counterpart—the electronic transistor—we have considered it appropriate to call it a *photonic transistor* (PT).

As far as practical realization of such a switching device is concerned, at the present time the best candidate for the role as a photonic transistor is an optical semiconductor device that is similar to a semiconductor optical amplifier (SOA). The SOA can handle multiple optical signal inputs, optical signal control, and is capable of implementing both wavelength and intensity signal switching functions at its output. Its applications to the construction of binary Boolean logic gates^{4,5} using wavelength switching and conversion^{6–15} are well known in the literature, as well as its applications as an electronically controlled photonic gate.¹⁶

Under these circumstances, we present below a photonic transistor configuration based on a wideband traveling wave SOA structure.^{16,17} The photonic transistor is controlled by an optical signal, and its operation as an optical signal intensity switch is based on the cross-gain modulation (CGM) properties of the underlying SOA structure. As will become clear shortly, the advantage of using this type of PT configuration over the more traditional optical gate configurations (e.g. Ref. 16) resides, on the one hand, in the fact that one can implement the intensity switching functions more accurately in terms of the shape of the output signal in the time domain. On the other hand, it will be shown that at the practical level the operation of the PT as an optical gate can be achieved by using SOA structures with smaller sizes than the typical SOA structures in use today, hence opening the possibility for on-chip integration of such PTs for the construction of the various configurations necessary for the practical implementation of NDP logic systems, as well as for other digital optical applications.

2.1 Functional Description of the Photonic Transistor

The functional configuration of the photonic transistor is depicted in Fig. 1. As can be seen from this figure, the photonic transistor consists of a semiconductor core that is similar in structure to a wideband traveling wave SOA

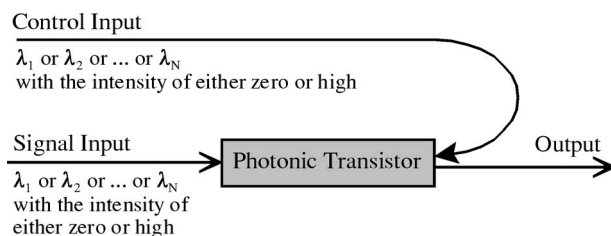


Fig. 1 The configuration of the photonic transistor.

structure with two input and one output ports. The logic symbol for the N-nary PT is shown in Fig. 2.

The two input ports of the PT, identified as the control signal (CS) input port and data signal (DS) input port have the following functional descriptions. Both these input ports take optical input signals with wavelengths $\lambda_i \in S(\lambda_1, \lambda_2, \dots, \lambda_N)$, where $S(\lambda_1, \lambda_2, \dots, \lambda_N)$ is a set of the wavelengths within the bandwidth of the PT and intensities that can either be “high” (a predetermined high intensity level in the system), or “low” (dark or a predetermined low intensity level in the system). By modulating of the intensity of the signal applied to the CS port, and by making use of the CGM properties of the semiconductor core, one can achieve at the output signal (OS) port of the PT the modulation of the intensity of the signal applied to the DS port that corresponds to the modulation of the control signal.

From the above considerations it follows immediately that in fact the two inputs of the PT can be used to implement a logic switching function at the output port of the transistor as follows: if one applies to the DS port of the device an optical signal with wavelength λ_i and on the CS port an optical signal of wavelength λ_j with $\lambda_i, \lambda_j \in S(\lambda_1, \lambda_2, \dots, \lambda_N)$, then the optical signal at the OS port will either be identical (in both intensity and wavelength) with the DS signal if the intensity of the CS signal is at low, or will be at low if the intensity of the CS signal is at high.

It should be noted that in the general case wavelengths λ_i, λ_j of the optical signals applied to the DS and CS ports of the PT need not be the same. However, in the special case when only one wavelength is used ($N=1$), the implementation of the switching function described above reduces the N-nary PT to a traditional Boolean binary logic gate.

It is also worth mentioning that the operation of the PT configuration as described above is analogous to that of a traditional electronic transistor where the output is switched ON to the signal input by the control input. The only difference in the operation of the traditional electronic transistor and the PT is due to the fact that while in the former

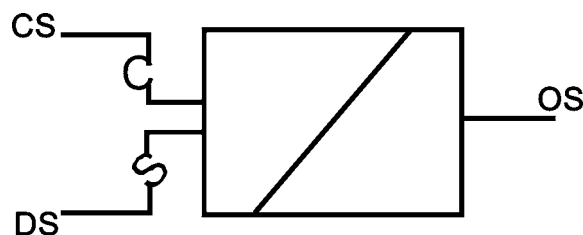


Fig. 2 The logic symbol of the photonic transistor.

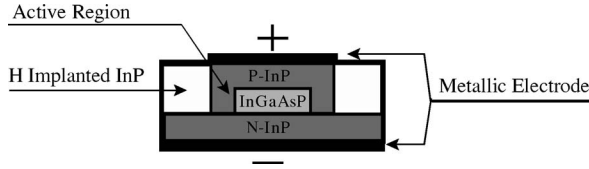


Fig. 3 The transistor design.

case, the ON operation of the switch is attained for a high value of the control input, in the latter case of the PT the ON operation corresponds to a low value of the signal at the CS port; i.e., the PT can be thought of as an “inverted” counterpart of the electronic transistor. This operational difference, however, has no impact on the switching performance of the PT, and for this reason we will continue to refer to it as a transistor.

2.2 Physical Description of the Photonic Transistor

As mentioned earlier, the physical structure underlying the design and operation of the PT has been chosen to be that of a wideband traveling wave SOA. The model that will be used to describe the operational characteristics of the PT was originally developed for a traditional InP/InGaAsP/InP buried stripe SOA,^{16,17} and in all of the following we will continue to use this configuration as the fundamental material configuration for the design of the PT. A cross-sectional view of this configuration is presented in Fig. 3, while Fig. 4 shows the dimensional details of the optically active core of the PT.

According to the functional description of the PT in the previous section, the optical signals of wavelength λ_i , $\lambda_j \in S(\lambda_1, \lambda_2, \dots, \lambda_N)$ injected into the embedded InGaAsP active core through the input coupling facet are amplified by coupling to the structure of the active region, and the resulting signal exits through the opposite output coupling facet. Inside the active region, neglecting transverse variations in the photon rates and carrier densities, each input signal of wavelength λ_k can be resolved into two traveling waves $E_k^{(\pm)}$ propagating in opposite directions obeying the differential equations:

$$\frac{dE_k^{(\pm)}(x)}{dx} = \left\{ \mp j\beta_k \pm \frac{1}{2} [\Gamma g_m(\lambda_k, n) - \alpha(n)] \right\} E_k^{(\pm)}(x), \quad (1)$$

where x is the longitudinal coordinate along the length L of the active region in Fig. 4, $j = \sqrt{-1}$ is the complex imaginary unit, β_k is the propagation vector corresponding to the signal of wavelength λ_k , Γ is the optical confinement factor of the structure, $g_m(\lambda_k, n)$ is the material gain coefficient of the

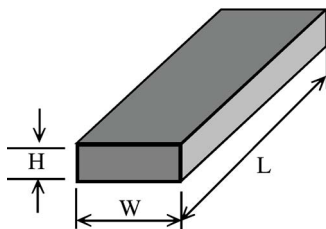


Fig. 4 The dimension of the active core.

active region, n is the charge carrier (electrons) density, and $\alpha(n)$ is the material loss coefficient of the active structure. The fields in Eq. (1) are, of course, subject to boundary conditions at the ends $x=0$ and $x=L$ of the active region, and these boundary conditions are

$$E_k^{(+)}(0) = (1 - r_1)E_k^{\text{in}} + r_1E_k^{(-)}(0),$$

$$E_k^{(-)}(L) = r_2E_k^{(+)}(L), \quad (2)$$

where E_k^{in} is the input signal of wavelength λ_k at the input facet located at $x=0$, and r_1, r_2 are amplitude reflectivity coefficients of the input and output facets, respectively.

As can be seen from Eq. (1), the constitutive equations for the traveling fields inside the active region depend strongly on the density of carriers $n(x)$ in this region, in the sense that it is the carrier density that controls the gain and losses of the signals as they pass through the active region. That this is indeed the case can be easily understood if we change our description of the phenomenology from fields to photon rates. To each of the fields $E_k^{(\pm)}$ one can associate a photon rate $N_k^{(\pm)}$ through the relations $N_k^{(\pm)} = |E_k^{(\pm)}|^2$, representing the number of photons (with wavelength λ_k) time crossing a transversal section of the active region per unit time. Under these circumstances, at each point along the length of the active region, the charge carrier density at each instant of time will be determined by the balance between the carriers injected into the active region by the bias current of the SOA and the loss of carriers through the various mechanisms that are relevant for the structure under consideration. In the case of the InGaAsP material, the losses mechanisms are due mainly to in-band recombination phenomena, which can be either independent of the photons present in the material (spontaneous in-band carrier recombination) or assisted by the these photons (photon assisted recombination), such that the variation of the carrier density at each point along the length of the active region can be described by the following rate equation:

$$\begin{aligned} \frac{dn(x)}{dt} = & \frac{I}{eHLW} - R[n(x)] \\ & - \frac{\Gamma}{HW} \sum_{k=1}^{N_s} g_m(\lambda_k, n(x)) [N_k^{(+)}(x) + N_k^{(-)}(x)] \\ & - \frac{2\Gamma}{HW} \sum_{j=0}^{N_m-1} \{g_m(\lambda_j, n(x)) K_j [N_j^{(+)}(x) + N_j^{(-)}(x)]\}, \quad (3) \end{aligned}$$

where in the right-hand side of Eq. (3), I is the bias current of the structure (assumed to have a uniform distribution in the active region), $R[n(x)]$ is the radiative and nonradiative overall spontaneous recombination rate (including two-particle, Auger, and leakage recombination phenomena), $N_k^{(\pm)}(x)$ are the photon rates, which can be shown to obey inside the active region constitutive equations similar to Eq. (1), N_m is the number of resonances of the active region seen as a resonant cavity, and K_j ($j=0, \dots, N_m-1$) is a normalization factor for the optical noise associated with each resonance of the cavity.

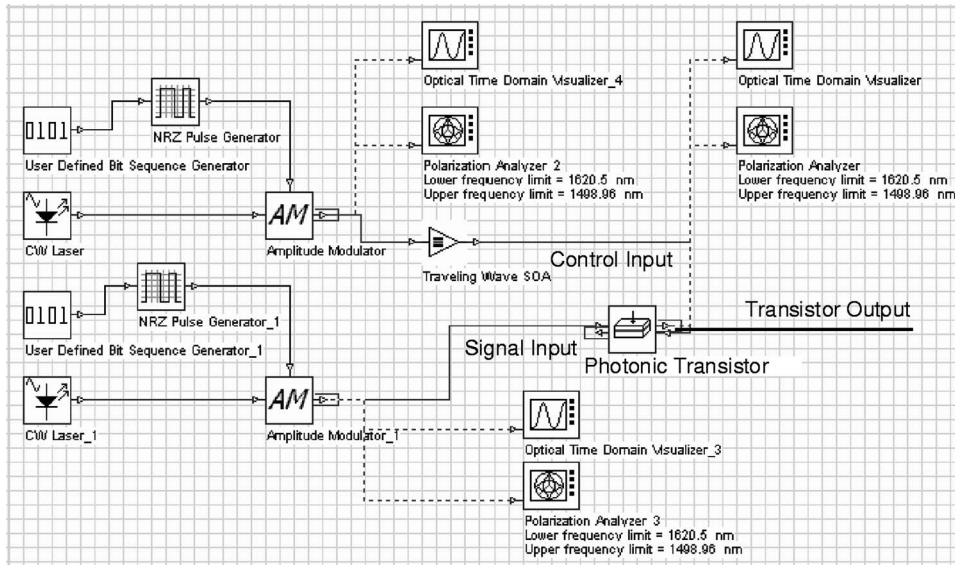


Fig. 5 The transistor simulation circuit.

For reasons that will become clear shortly, our investigation requires the explicit ability to account for the influence of the size of the active region—and in particular the effects of size reduction—on the operation and performance of the PT. However, in order to be able to do so, it is necessary to first identify and appropriately control all the parameters and physical quantities of the model that have an explicit dependence on the size of the active region. This additional precaution is necessary because the model itself does not exhibit explicitly the full dependence of all the parameters and physical quantities involved on the size of the active region. A perfect illustration of this latter feature of the model is given by Eq. (3): while the carrier density has a visible functional dependence on the dimensions of the active core as described by the rate equation, this is by no means its full functional dependence on these dimensions. The carrier density has also a hidden dependence on the size of the active region through a parameter that in this model (and its software implementation) appears only as a numerical input factor; i.e. through the optical confinement factor Γ . Of course, similar arguments apply to all the equations, parameters, and physical quantities involving the confinement factor Γ , and for this reason, in order to be able to investigate the size effects on the performance of the SOA switch, one needs to specify the relation between the confinement factor and the dimensions of the active core.

One of the standard relations between the optical confinement factor Γ and the dimensions of the active core comes from the theory of laser diodes and is given by the expression:¹⁸

$$\Gamma = \frac{D^2}{D^2 + 2}, \tag{4}$$

where D is the normalized thickness of the active layer:

$$D = 2\pi \left(\frac{H}{\lambda} \right) \sqrt{n_A^2 - n_E^2}, \tag{5}$$

with H the thickness of the active region, λ the wavelength of the radiation passing through the active region, n_A the optical refractive index of the active region and n_E the optical refractive index of the material embedding the active region (in Fig. 3, $n_E=3.167$ is the refractive index of the InP layer surrounding the InGaAsP active core with refractive index $n_A=3.22$). It should be noted at this time that while Eqs. (4) and (5) do not constitute, strictly speaking, an exact expression for the optical confinement factor, they are compatible with the model described above and they

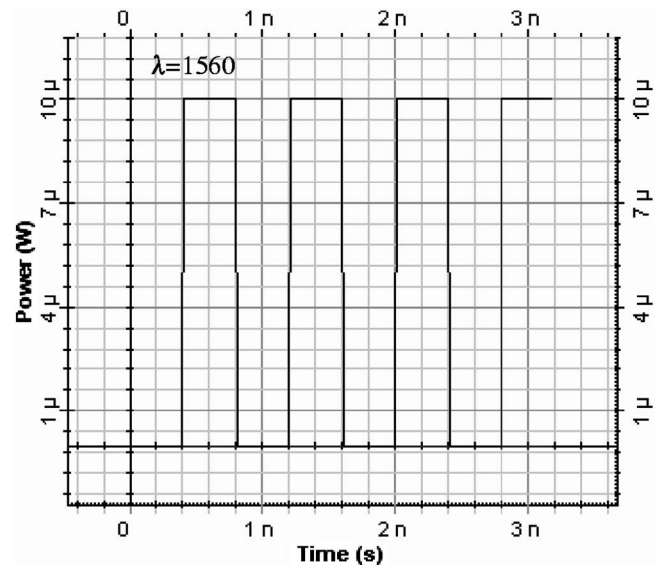


Fig. 6 Control input signal ($\lambda=1560$ nm).

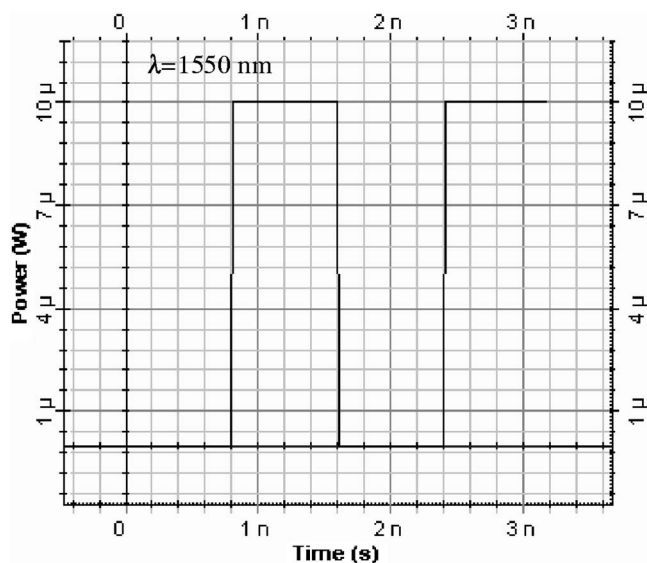


Fig. 7 Data input signal ($\lambda = 1550$ nm).

offer numerical values for Γ that are accurate enough for our present purpose.

As for the numerical investigation of the PT, all our numerical work has been carried out by using a commercially available simulation software—the OPTISYSTEM simulation package¹⁹—which is based explicitly on the model described above.²⁰ The numerical implementation of the model in the OPTISYSTEM simulation software uses finite-difference methods for solving the partial differential equations of the model with the appropriate boundary conditions, and follows closely the procedures described in Refs. 16 and 17 to simulate both the steady-state and the fully dynamic regimes of operation of the PT.

Prior to the use in the present work, the OPTISYSTEM simulation package has been subjected by the authors to extensive and meticulous testing. The results of this testing have shown that it reproduces with excellent accuracy the SOA data currently available in the literature, justifying its use in the present work.

2.3 Practical Design Considerations

In order to make the PT practically useful, especially for on-chip integrated photonic circuitry, the practical/physical design of the PT must satisfy several important requirements: (1) it should be wideband so that a large number N of wavelengths can be used, (2) it should have small physical dimensions as to allow for the on-chip integration, (3) it should have low power consumption so that the total power consumption of the chip can be manageable, and (4) it should be compatible with future PT and waveguide integration.

The first of these requirements has already been taken into consideration by the previous choice of the optical amplifier structure as the underlying structure for the design of the PT. The remaining three requirements, however, are closely linked to each other and require more detailed consideration.

The second of the above requirements, which involves adjusting the size of the PT to values appropriate for on-

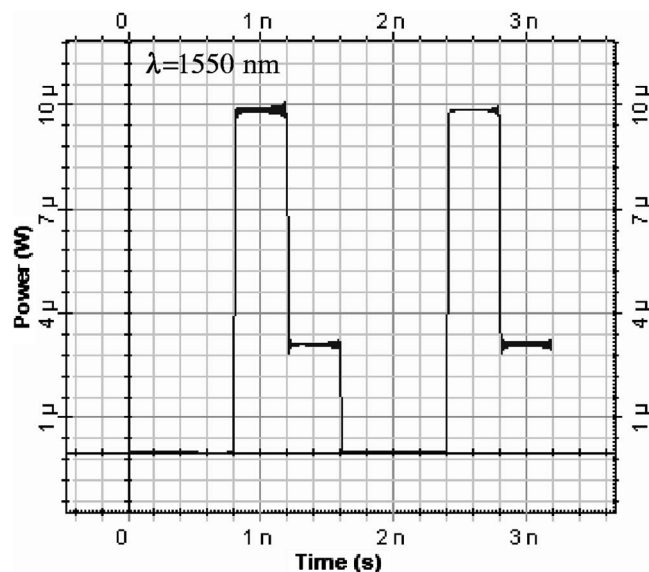


Fig. 8 The output signal of the photonic transistor ($\lambda = 1550$ nm).

chip integration, is perfectly feasible to be put into practice. Indeed, with the current technology it is possible to manufacture optical amplifiers with sizes ranging from submillimeter scale to nanometer scale, using a variety of techniques from selective metal-organic vapor-phase epitaxy²¹ and metal-organic chemical vapor deposition²² to reactive ion etching²³ and molecular beam epitaxy.²⁴ Furthermore, and even if at the present time it covers mostly the micrometer range in terms of the size of the structures involved, the on-chip integration of optical amplifiers has been successfully realized in practice for a variety of configurations (e.g., Ref. 25). Under these circumstances, and as much as size is concerned, the practical implementation of this requirement does not impose any insurmountable

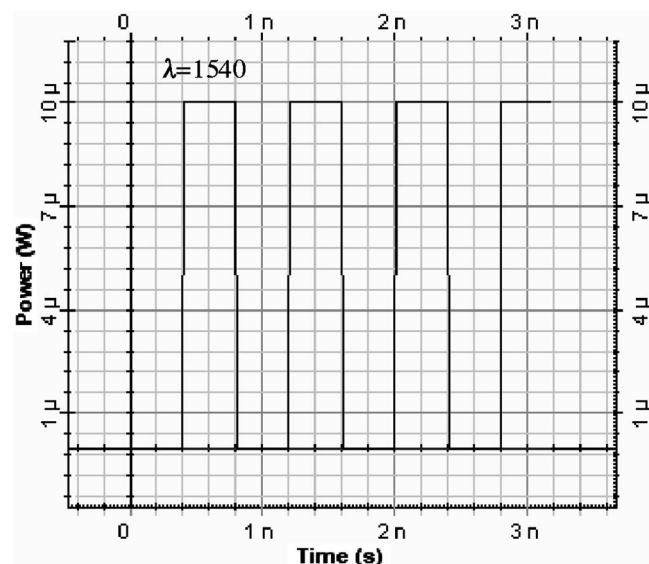


Fig. 9 Control input signal with wavelength of 1540 nm.

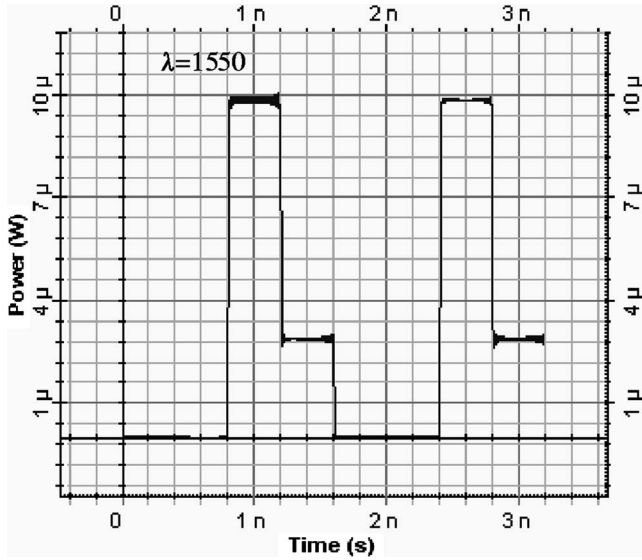


Fig. 10 The output signal of the photonic transistor ($\lambda=1550$ nm).

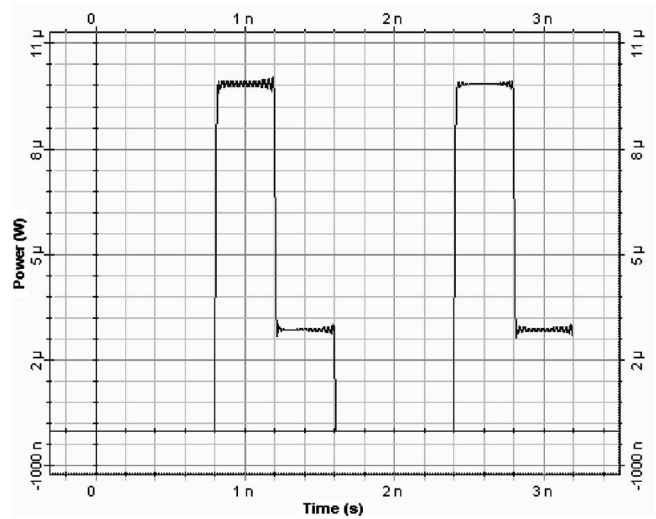


Fig. 11 The output signal of the photonic transistor ($\lambda=1550$ nm).

challenges and is achievable at submicrometer scale at the very least even with the present level of technological knowledge.

Size reduction is not only beneficial for on-chip integration by allowing one to incorporate a larger number of PT structures on one chip, but it is also closely linked to the third requirement above, regarding the power levels that are necessary to operate such devices. For a given material structure, as the dimensions of the PT/active core are decreased, the power consumption required for the operation of the device also decreases in accordance to the limits imposed by size. Furthermore, in theory (and similar to the case of electronic semiconductor devices), the smaller the size of the device, the higher is its performance in terms of power consumption and operational speed.

The above considerations suggest that size reduction is an essential and deciding factor not only in the practical realization and integration of the PT, but also for the performance level of its operation. However, while this is true in the near-micrometer size range and above, one must take into consideration the fact that as the dimensions of the active core of the PT are reduced below a certain size level, its performance will be affected—at least quantitatively if not also qualitatively—by quantum effects that become dominant.

Table 1 The truth table of the N-nary O-AND.

Signal input	Control input	PT output
0	0	0
0	λ_j	0
λ_j	0	0
λ_j	λ_j	λ_j

Generally speaking, there is no clear dimensional delimitation that separates the classical and quantum regimes of operation of semiconductor devices. This statement must be understood in the sense that while dimensional scales at which the behavior of the corresponding semiconductor devices is classical or quantum are well known, these scales are not entirely disjoint and overlap in the submicrometer to nanometer range. Things become even more complicated when one takes into account the fact that the mathematical models describing the properties and/or operation of semiconductor structures are never “purely classical” or “purely quantum.” Indeed, most of the current models in solid state physics and engineering are “semiclassical,” incorporating to various degrees both classical and quantum concepts (e.g., classical electromagnetic fields and the band structure of solids, quantum cross sections for the various interaction processes, etc.).

Under these circumstances, the classical and quantum regimes for the operation of semiconductor devices with sizes within the above overlap range become that much harder to recognize. At the same time and as far as dimensionality is concerned, the validity domain of a model used to describe the operation of a semiconductor device becomes less dependent on a specific size that separates classical from quantum and more dependent on the model itself and on how and which classical and quantum concepts it incorporates.

Table 2 The truth table of the binary O-AND as a special case.

Signal input	Control input	PT output
0	0	0
0	λ_j	0
λ_j	0	0
λ_j	λ_j	λ_j

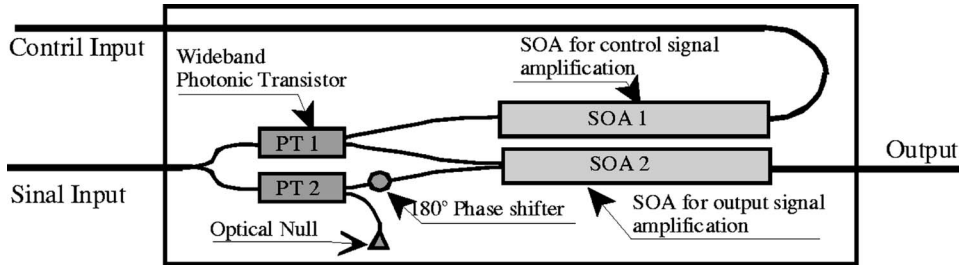


Fig. 12 The O-AND gate construction using photonic transistors.

As far as the model used in this work and its dimensional validity are concerned, the model is semiclassical,^{16,17} combines (interchangeably) the classical concept of guided electromagnetic fields with the quantum concept of photons, and takes explicitly into account the energy band structure of the underlying semiconductor materials, the mass renormalization effects on the charge carriers, the cross sections/relaxation times of the various linear and nonlinear interaction processes involved, etc. Since most of the quantum features of the model are less related to the size of the active core of the PT and more dependent on its material structure, and since the classical electromagnetic description is well-known to be reasonably accurate in the molecular range,²⁶ we expect the dimensional validity range of the model to extend well below the submicrometer scale. Under these circumstances, while our numerical results based on this model may not be completely accurate quantitatively for the sizes of the structures under consideration in the present work, we do expect them to be qualitatively accurate and hence representative for the switching operation of the PTs with sizes in this range.

3 Numerical Investigation of the Photonic Transistor

The PT design described in the previous section was tested by computer simulations. The theoretical background of the numerical method can be found in Ref. 17. Figure 5 is the circuit used for the simulations. The names of the components are shown in the figure. The data signal is generated by a CW laser, an electrical domain pulse generator, and an amplitude optical modulator. The wavelength and the intensity of the signal required for the simulation are inputs of the CW laser component. The bit rate required for the simulation is set in the bit sequence generator. The control input signal is produced in the same manner. The wavelengths for the signal input and the control input is set independently in

Table 3 The standard binary form for the binary O-AND gate.

Signal input	Control input	PT output
0	0	0
0	1	0
1	0	0
1	1	1

each given simulation case, which allows for the simulation of the entire band of the device. Monitoring devices, such as optical time domain visualizers and polarization analyzers are attached to the output of the modulators. In the simulations we use these devices to inspect the input signals. The dimension and material related factors are the inputs of the wideband traveling wave SOA module. By changing these input parameters, we can simulate different devices with various dimensions. The simulations discussed in the following section utilize the microstructure of the SOA module, but the sizes used are smaller since we use the structure for transistor functionality.

As shown in Fig. 5, the control signal is amplified by a traveling wave amplifier for the purpose of creating a power bias between the signal input and the control input. This bias causes a higher cross-gain modulation, resulting in a lower transistor output for the low logic output case. As mentioned earlier, the ideal low output power would be zero. However, the low output logic is produced by the cross-gain modulation effect of the structure and as a result it is very difficult to reach absolute zero. Although a non-absolute-zero transistor can be used to construct logic gates, a low output closer to zero is more desirable and will make a better transistor.

Also shown in Fig. 5, the output of the simulation is measured by the optical time domain visualizer that records the intensities of the signal in the time domain. The polarization analyzer is used to monitor the polarization angles of the signal. Although we simulated several different operational configurations, corresponding to different core sizes and signal power levels, we present below three of the most relevant examples.

3.1 Simulation Example 1

In this example, we simulated the PT that has an active core with the dimension of $H=50$ nm, $W=100$ nm, and $L=1000$ nm. The input power required by the PT in order to produce the logic function is around 5 mW, which was used in the simulation. The control input is generated by a

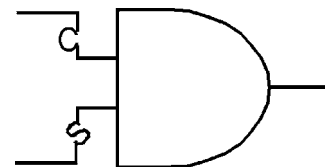


Fig. 13 The logic symbol of the O-AND gate.



Fig. 14 The logic operator for the O-AND gate.

bit generator and an amplitude modulator, as shown in Fig. 5. The bit sequence is set 01010101. The corresponding control signal is shown in Fig. 6. The wavelength for the modulator is produced by a pump laser, which was chosen as 1560 nm in this case. A traveling wave SOA is inserted into the control input line to amplify the signal intensity in order to produce a power bias between the control input and the signal input to the transistor. The power bias helps to lower the logic low output of the transistor, to make it easier for using the transistor to construct logic gates.

The data signal input is generated by a bit generator and an amplitude modulator as well, also shown in Fig. 5. The bit sequence was chosen as 00110011, in order to produce all of the possible combinations between the control input and the signal input. The wavelength for the signal input was chosen as 1550 nm. The corresponding signal waveform is shown in Fig. 7. The output of the transistor is shown in Fig. 8. The wavelength of the output is identical to the signal input, which is 1550 nm in this case.

By comparing the control input and the data input with the output signals, we can see that the PT produces the required transition functions, i.e., when the control input is at zero, the output equals the signal input, while the control input is at high and the output is at low. As examples, when the time is at 1 ns, the control input signal is at zero, refer to Fig. 6; for the case in which the signal input is at high, refer to Fig. 7; for the case in which the PT output is at high, refer to Fig. 8. When the time is at 1.4 ns, the control input is at high, the signal input is also at high, but the PT output is at low.

From Fig. 8, we see that the low of the PT output is about 30% of the high. Ideally, we would like to have the low at zero. However, due to the fact that the output low is produced by the cross-gain modulation mechanism of the

heterostructure, it is very hard to achieve the output of zero. A structural absorber can be attached to the PT output to further bring the low to zero. However, it is not always needed, since the “not-at-zero” low can be further manipulated when using the PT to construct logic gates, so that the output of the gates will be at either high or zero for each of the light waves used in the system. This will be discussed in the following section.

3.2 Simulation Example 2

In order to test the bandwidth of the transistor, a second experiment was simulated in which the wavelength of the control signal is changed to 1540 nm, while keeping the signal input to the transistor at the same wavelength of 1550 nm. Figure 9 is the control signal waveform and Fig. 10 gives the output signal of the transistor. It can be seen that the output signal maintained the same intensity as of the previous test case in which the control input had a wavelength of 1560 nm. This tells us that the transistor design has at least 20 nm of bandwidth, from the range of 1540 to 1560 nm. We can, therefore, choose N number of wavelengths within the range of 1540–1560 nm for the NDP system, if this transistor is used to construct the N-nary photonic logic gates. The band gap between the wavelengths is determined by the I/O devices of the system. If we use a 0.8 nm gap, as is used in some dense wavelength division multiplexing (DWDM) systems, this transistor will provide around 20 wavelengths for information encoding and processing.

3.3 Simulation Example 3

The same experiment is applied to a very small transistor with the dimension of $H=10$ nm, $W=20$ nm, and $L=1000$ nm. The same data and control signal patterns used in the large size simulations are used again in this case. The wavelengths for the data signal and the control signal are both 1550 nm in this simulation.

The result is shown in Fig. 11. It is noticed that the power required by this transistor is much smaller, only $10 \mu\text{W}$. The signal is also cleaner, which indicates the

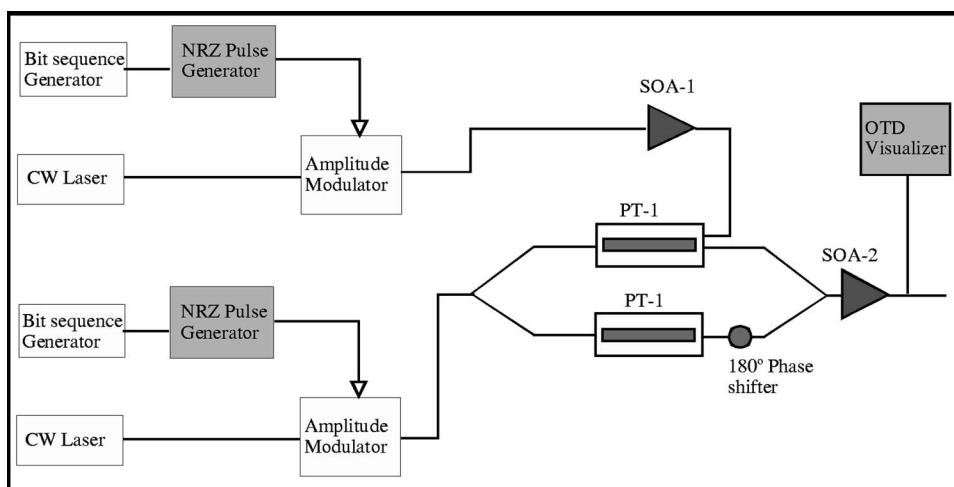


Fig. 15 The O-AND gate simulation circuit.

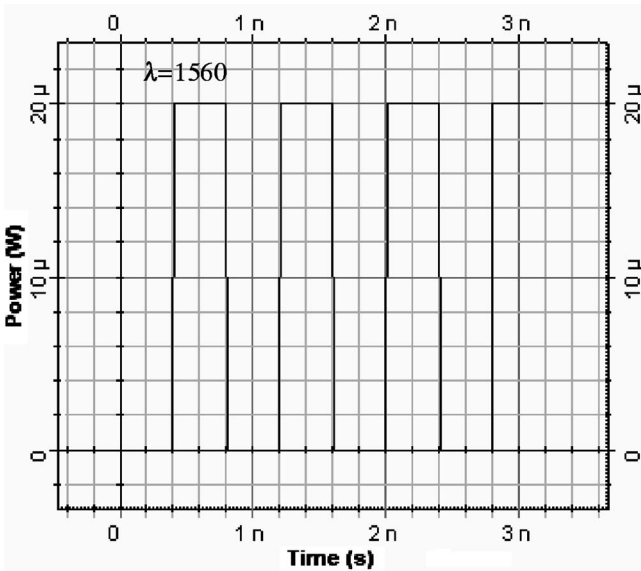


Fig. 16 The signal input of the O-AND gate.

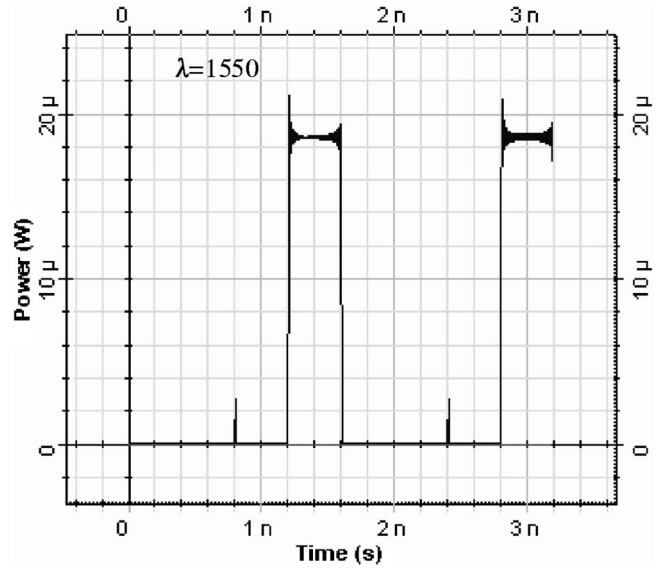


Fig. 18 The O-AND gate output.

speed of this very small transistor is higher. Further studies on the speed of the transistor are ongoing and will be reported in future publications.

Regarding the accuracy of the simulation for Example 3, one might argue the quantum effect. However, we have seen consistent results from large sizes to very small sizes. Therefore, we believe that the results for this case are still in a reasonably accurate range, although the quantum effect may have some influence.

4 Applications

As mentioned earlier, the above discussed photonic transistor can be used to construct logic gates. As an example, we use the PT to construct an N-nary optical AND (O-AND) gate. The logic functions of the N-nary O-AND gates are defined as follows: If the control input is a zero (dark), the

output will be zero; but, if any λ_i with $\lambda_i \in S(\lambda_1, \lambda_2, \dots, \lambda_N)$ presents on the control input, the output will be equal to the data signal input. Table 1 is the truth table of the O-AND gate. It is worth noting that the N-valued digital logic system is not symmetric, unlike Boolean logic. We cannot switch the roles of the control input and the data input at the gate level in the NDP system. However, when only one wavelength is used, the O-AND gate not only becomes symmetric but also, importantly, becomes the standard Boolean binary logic AND gate. The truth table is given by Table 2. Since only one wavelength is used in the binary case, we can use the high intensity to represent 1 and the zero intensity to represent 0. Under these circumstances, Table 2 can be rewritten into the standard binary format as shown in Table 3.

Figure 12 shows the design of the N-nary O-AND gate, in

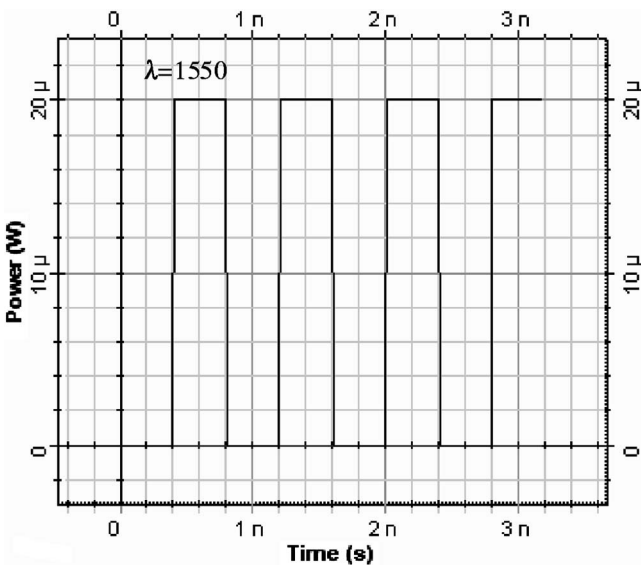


Fig. 17 The control input of the O-AND gate.

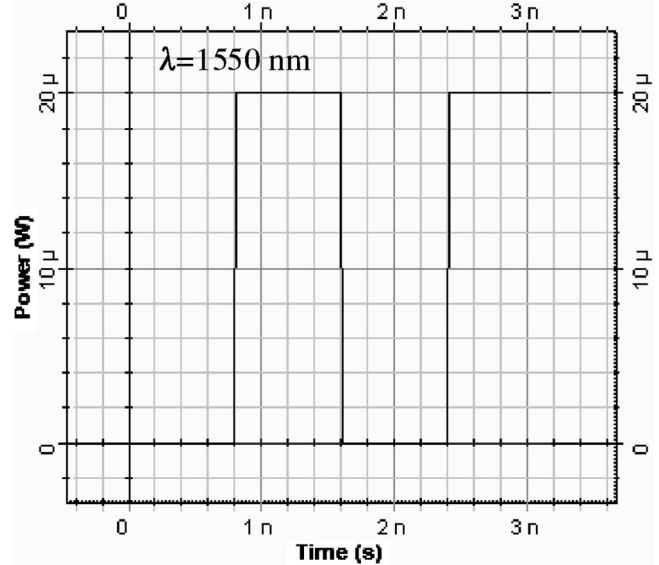


Fig. 19 The O-AND control input ($\lambda=1550$ nm).

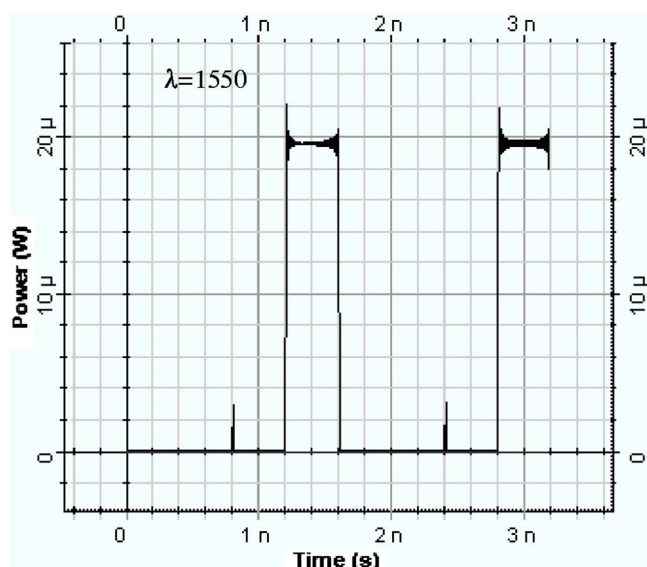


Fig. 20 The binary O-AND gate output.

which two PTs and two SOAs were used. The control signal to PT-1 is amplified by SOA-1 to create a power bias between the signal input and the control input to produce high cross-gain modulation within PT-1, in order to make the low output sufficiently low. PT-2 is identical to PT-1, in order to form a Mach-Zehnder interferometer. The control input of PT-2 is set at a constant zero, along with an 180 deg phase shifter, makes the Mach-Zehnder interferometer formed by PT-1 and PT-2 have a destructive recombination at the output. This destructive recombination of the Mach-Zehnder interferometer cancels the high output of PT-1, resulting in the output of the O-AND gate as defined in Table 1. SOA-2 is used to amplify the output signal to reach the same level as of the input which is 20 μ W in this case.

It is worth noting that the O-AND gate design shown in Fig. 12 uses two PTs in a Mach-Zehnder structure to produce the required logic function. This design eliminates the “side effect” of the not-at-zero low of the PT, since it is the difference between PT-1 and PT-2 that produces the high output of the O-AND gate when both the data input and the control input are high (see row number 4 in Tables 1 and 3). In other words, this design produces an ideal low (at zero) at the gate level although the PT itself has a non-ideal not-at-zero low. Figure 20 illustrates the output of the O-AND gate, showing the zero logic low.

It is also interesting to know that we have observed zero output in a laboratory experiment using a standard SOA when we inject high intensity inputs at both the data input and the control input. This is somehow related to the total saturation of the SOA, in our view, when the combined intensity of the control and data signals reach at a certain level. However, the numerical model used in our simulation discussed earlier does not build in the algorithm or the capability to model this condition. Further research is needed both theoretically and experimentally to investigate the phenomena, as it is important to use this in designing ideal low output PTs.

The logic symbol of the O-AND gate is shown in Fig. 13.

Similar to the photonic transistor symbol, a “C” and an “S” are put on the inputs to signify control and signal inputs, respectively. However, when only one wavelength is used, the N-nary O-AND gate becomes a binary O-AND gate, in which case, the O-AND gate is symmetric. This means that one signal can be the control of the other, in exactly the same manner as Boolean logic.

Figure 14 shows the operator symbol of the O-AND gate. A big “O” circles around the AND signifies optical to distinguish from the electrical AND.

The logic symbol, shown in Fig. 13, can be used in photonics circuit designs in the same manner as the electrical AND gate symbol in electronics circuits. The logic operator, shown in Fig. 14, can be used in mathematical logic manipulations in the same manner as those used the Boolean algebra.

The O-AND gate design shown in Fig. 12 was simulated using the OPTISYSTEM software. Figure 15 is the circuit for the simulation. The components of the circuit are labeled in side the figure. The input and output signals are measured by the Optical Time Domain (OTDM) Analyzer, as shown in Fig. 15. The polarizations of the signals were also monitored by the polarization analyzers during the simulations.

Figure 16 is the signal input for the O-AND gate, which is generated by an amplitude modulator powered by a 1550 nm CW laser. Figure 17 is the control input to the O-AND gate, which has the wavelength of 1560 nm. The output signal of the O-AND gate is given in Fig. 18. The result matches the truth table of the O-AND gate shown in Table 1.

The binary case, when only one wavelength is used, was also tested at $\lambda=1550$ nm. The same control signal of 1550 nm wavelength, shown in Fig. 17, was used. The signal input of 1550 nm is shown in Fig. 19. The output of the binary O-AND gate is given by Fig. 20. It can be seen that the result displays a Boolean binary logic AND.

5 Conclusions

In the present paper we have investigated a new optoelectronic device called an N-nary photonic transistor (PT), as well as its application to the construction of digital O-AND gates. Our numerical investigation of the PT and of the digital gate produced satisfactory results for the operational performance of both the PT and the O-AND gate.

As part of the investigation of the performance of the PT, we have also studied the role played by the size of the active core in its operation. Our results indicate that within the limitations imposed by the model that was used in the simulation of the PT, the reduction of the size of the active core improves the performance of the device in terms of both of power consumption and speed, similar to the case of standard electronic transistors.

Since the model used in the numerical analysis is semi-classical, we are confident that our results are accurate—qualitatively at the very least—for sizes down to tens of nanometers. A version of the present model that takes into account more explicitly the quantum effects arising from the size reduction below the sizes mentioned above is currently under development and testing, and the results of its application to the study of the PT configuration will constitute the subject of a future publication.

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